In the claims:

Following is a complete set of claims as amended with this Response.

1. (Currently Amended) A circuit comprising:

a plurality of memory modules;

a memory controller coupled to the plurality of memory modules;

a resistive bus splitter ~~plurality of bus splitters~~ coupled between the plurality of memory modules and the memory controller to split signals communicated between the plurality of memory modules and the memory controller, the resistive bus splitter having a specific resistance for each memory module; and

a plurality of terminators to reduce signal reflections corresponding to the split signals.

2. (Original) The circuit of claim 1 wherein the plurality of terminators are embedded in each of the plurality of memory modules.

3. (Original) The circuit of claim 1 wherein the plurality of terminators are embedded in the memory controller.

4. (Original) The circuit of claim 1 wherein the memory modules are dual in-line memory modules (DIMMs).

5. (Original) The circuit of claim 1 further including a reference voltage generator to generate a reference voltage corresponding to a memory chip voltage.

6. (Original) The circuit of claim 5 wherein the reference voltage is provided to the plurality of memory modules and the memory controller.

7. (Currently Amended) The circuit of claim 1 wherein the resistive bus splitter includes ~~plurality of bus splitters are one or more items selected from a group comprising miniature resistive splitters on a PCB and~~ miniature integrated resistor packs.

8. (Currently Amended) The circuit of claim 1 further including a plurality of memory expander chips (MXCs) coupled between the resistive bus splitter ~~memory controller~~ and the plurality of memory modules.

9. (Currently Amended) The circuit of claim 8 wherein the plurality of MXCs include a micro-controller to perform tasks locally ~~enable access to relative larger memory arrays~~.

10. (Currently Amended) The circuit of claim 8 wherein each of the plurality of MXCs include ~~one or more items selected from a list comprising a micro-controller to perform tasks locally and~~ a built in bi-directional cache to decrease latency and increase throughput efficiency.

11. (Original) The circuit of claim 8 wherein a data rate between the memory controller and the plurality of MXCs runs at a relatively higher bandwidth than that of directly supported DIMMs.

12. (Original) The circuit of claim 8 wherein each of the plurality of MXCs include functionality selected from a group comprising local refresh generation, dynamic address space re-mapping, access re-ordering, access coalescing, memory power-on self-test (POST), and local management of open pages.

13. (Original) The circuit of claim 8 wherein a portion of the plurality of MXCs are coupled to each other in series.

14. (Currently Amended) A method comprising:

~~providing a plurality of memory modules;~~

sending address signals from ~~coupling~~ a memory controller to a ~~the~~ plurality of memory modules through a resistive bus splitter;

splitting the address ~~coupling a plurality of bus splitters between the plurality of memory modules and the memory controller to split~~ signals communicated between the plurality of memory modules and the memory controller at the resistive bus splitter;

providing a specific resistance to the address signals for each memory module at the resistive bus splitter; and

terminating the address signals ~~providing a plurality of terminators~~ to reduce signal reflections corresponding to the split signals.

15. (Currently Amended) The method of claim 14 wherein terminating comprises terminating at ~~the plurality of~~ terminators ~~are~~ embedded in each of the plurality of memory modules.

16. (Currently Amended) The method of claim 14 wherein terminating comprises terminating at ~~the plurality of~~ terminators ~~are~~ embedded in the memory controller.

17. (Original) The method of claim 14 wherein the memory modules are dual in-line memory modules (DIMMs).

18. (Currently Amended) The method of claim 14 further including generating a reference voltage corresponding to a memory chip voltage and providing the reference voltage to the plurality of memory modules and to the memory controller.

19. (Currently Amended) The method of claim 18 wherein the resistive bus splitter includes a miniature resistive splitter on a PCB ~~reference voltage is provided to the plurality of memory modules and the memory controller~~.

20. (Currently Amended) The method of claim 14 wherein the resistive bus splitter includes ~~plurality of bus splitters are one or more items selected from a group comprising miniature resistive splitters on a PCB and~~ miniature integrated resistor packs.

21. (Currently Amended) The method of claim 14 sending address signals further includes sending the address signals through ~~further including coupling~~ a plurality of memory expander chips (MXCs) between the resistive bus splitter ~~memory controller~~ and the plurality of memory modules.

22. (Original) The method of claim 21 wherein the plurality of MXCs enable access to relatively larger memory arrays.

23. (Original) The method of claim 21 wherein each of the plurality of MXCs include one or more items selected from a list comprising a micro-controller to perform tasks locally and a built in bi-directional cache to decrease latency and increase throughput efficiency.

24. (Original) The method of claim 21 wherein a data rate between the memory controller and the plurality of MXCs runs at a relatively higher bandwidth than that of directly supported DIMMs.

25. (Original) The method of claim 21 wherein each of the plurality of MXCs include functionality selected from a group comprising local refresh generation, dynamic address space re-mapping, access re-ordering, access coalescing, memory power-on self-test (POST), and local management of open pages.

26. (Original) The method of claim 21 wherein a portion of the plurality of MXCs are coupled to each other in series.

27. (Currently Amended) A computer system comprising:

a central processing unit (CPU);

a graphics accelerator ~~display device~~ coupled to the CPU to generate ~~display~~ an image;

a plurality of memory modules;

a memory controller coupled to the plurality of memory modules and the CPU;

a resistive bus splitter ~~plurality of bus splitters~~ coupled between the plurality of memory modules and the memory controller to split signals communicated between the plurality of memory modules and the memory controller, the resistive bus splitter having a specific resistance for each memory module; and

a plurality of terminators to reduce signal reflections corresponding to the split signals.

28. (Currently Amended) The computer system of claim 27 wherein the resistive bus splitter includes miniature integrated resistor packs ~~further including a main memory coupled to the CPU~~.

29. (Currently Amended) The computer system of claim 27 further including a plurality of memory expander chips coupled between the resistive bus splitter and the plurality of memory modules to perform memory functions independent of the memory controller ~~memory coupled to the display device to store the image~~.

30. (Currently Amended) The computer system of claim 29 ~~claim 27~~ wherein the memory expander chip functions include at least one of refresh, dynamic address space re-mapping and memory power-on self-test (POST) ~~controller is coupled to the CPU through a memory control hub~~.